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AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the method comprising:

assigning the source logic to a first logic block in the PLD; assigning the destination logic to a second logic block in the PLD;

identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling to the solely the programmable routing multiplexer; STOCKSHIPP FOR THERE

routing the node on a first routing path between the first and second logic impatible the abded blocks, wherein the first routing path traverses the programmable routing multiplexer receive the destivia the first data input terminal; and hatharday committee

routing the node on a second routing path between the first and second logical brother and a blocks, wherein the second routing path traverses the programmable routing this wherein the second routing path traverses the programmable routing this was subjected to multiplexer via the second data input terminal.

2. (Currently Amended) The method of Claim 1, further comprising:

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identifying a third data input terminal of the programmable routing multiplexer, wherein a selection between the first and third data input terminals is determined solely by a second value stored in a second memory cell controlling the programmable routing multiplexer; and

routing the node on a third routing path between the first and second logic blocks, wherein the third routing path traverses the programmable routing multiplexer via the third data input terminal.

3. (Original) The method of Claim 1, wherein the PLD is a field programmable gate array (FPGA).

- 4. (Original) The method of Claim 3, wherein the first memory cell is a static RAM-based configuration memory cell of the FPGA.
- 5. (Original) The method of Claim 1, wherein the multiplexer is a 4-to-1 multiplexer.
- 6. (Original) The method of Claim 1, wherein the identifying, the routing the node on the first routing path, and the routing the node on the second routing path are performed interactively with each other.

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7. (Original) The method of Claim 1, further comprising:

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e targle where the evaluating the source and destination logic and determining that the source and مهم بالمعادة * destination logic do not forma portion of astriple modular redundancy (TMR) circuits المعادة الم

executable code for implementing addesign in a programmable logic device (PLD) to see the reduce susceptibility to single-event upsets (SEUs), the design comprising source and a mode coupled between the source logic and the action logic, the medium comprising:

code for assigning the source logic to a first logic block in the PLD and assigning the destination logic to a second logic block in the PLD; and code for:

identifying first and second data input terminals of a programmable routing multiplexer in the PLD, wherein a selection between the first and second data input terminals is determined <u>solely</u> by a value stored in a memory cell controlling the programmable routing multiplexer,

routing the node on a first routing path between the first and second logic blocks, wherein the first routing path traverses the programmable routing multiplexer via the first data input terminal, and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

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- 9. (Original) The computer-readable storage medium of Claim 8, further comprising code for evaluating the source and destination logic and determining that the source and destination logic do not form a portion of a triple modular redundancy (TMR) circuit.
- 10. (Currently Amended) A computer system for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the computer system comprising:

a placement module for assigning the source logic to a first logic block in the source logic block in the PLD; and the source logic block in the sou

identifying first and second data input terminals of a programmable and entering to the programmable and second as members of a programmable and second as members as the programmable routing multiplexer in the PLD, wherein a selection between the first and second as members as the management of the data input terminals is determined solely by a value stored in a memory cells of the second as the second as

blocks, wherein the first routing path traverses the programmable routing makes the multiplexer via the first data input terminal; and

routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

11. (Original) The computer system of Claim 10, further comprising an evaluation module for evaluating the source and destination logic and determining that the source and destination logic do not form a portion of a triple modular redundancy (TMR) circuit.

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12. (Currently Amended) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the method comprising:

generating a PLD placement wherein the source logic is assigned to a first logic block in the PLD and the destination logic is assigned to a second logic block in the PLD;

routing the PLD placement to generate a routed design wherein the node is routed on a first routing path between the first and second logic blocks, the first routing path traversing a programmable routing multiplexer via a first data input terminal of the an Mindago happrogrammable routing multiplexer; which has do governo dogs a benefit of the system of the large

en entre of the continuous identifying a second data input terminal of the programmable routing the continuous and the continuous areas of the x inale of a momultiplexer, wherein a selection; between the first and second data input terminals is to selection; between the first and second data input terminals is to selection; between the first and second data input terminals is tis butwice with determined solely by a first value stored in a first memory cell controlling the make or polet, but a fr researt werken sprogrammable routing multiplexers and randmarkeng before as a common of a series of the secretary

resident to the contingation in a second routing path between the first and second logic depaths in the c Angels for the blocks, wherein the second routing path traverses the programmable routing who make the blocks multiplexer via the second data input terminal materials and the 11.

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13. (Currently Amended) The method of Claim 12, further comprising:

identifying a third data input terminal of the programmable routing multiplexer, wherein a selection between the first and third data input terminals is determined solely by a second value stored in a second memory cell controlling the programmable routing multiplexer; and

routing the node on a third routing path between the first and second logic blocks, wherein the third routing path traverses the programmable routing multiplexer via the third data input terminal.

14. (Original) The method of Claim 12, wherein the PLD is a field programmable gate array (FPGA).

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- 15. (Original) The method of Claim 14, wherein the first memory cell is a static RAM-based configuration memory cell of the FPGA.
- 16. (Original) The method of Claim 12, wherein the multiplexer is a 4-to-1 multiplexer.
- 17. (Original) The method of Claim 12, further comprising:

 evaluating the node and determining that the node is not included in a triple
 modular redundancy (TMR) circuit.

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and the second less than the second to single-event upsets (SEUs), the design comprising source and the second logic, destination logic, and a mode coupled between the source logic and the second logic, the medium comprising source and the second logic, and a mode coupled between the source logic and the second logic and the second logic and the second logic logic.

routing path traversing a programmable routing multiplexer, and

code for performing post-processing of the routed design, comprising:

code for identifying a second data input terminal of the programmable routing multiplexer, wherein a selection between the first and second data input terminals is determined by a value stored in a memory cell controlling the programmable routing multiplexer, and

code for routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

- 19. (Withdrawn) The computer-readable storage medium of Claim 18, further comprising code for evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.
- 20. (Withdrawn) A computer system for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the design comprising source logic, destination logic, and a node coupled between the source logic and the destination logic, the computer system comprising:

a placement module for generating a PLD placement wherein the source logic is assigned to a first logic block in the PLD and the destination logic to a second logic rmenerality of block in the PLD; the control of a subserve design was not above on the control of the control of

the PLD placement to generate a routing module for routing the PLD placement to generate a routed design and the content of members become wherein the mode is routed on affirst routing path between the first and second logic of a particular and a was broke began data input terminal of the programmable routing multiplexemand recession in the broke more than the bree រង្វាម្ភាមិនដែលវិសាទៅ ជាជា**post-processing modülesfor**មានជនទៅនៃការការដែលនេះ មានសាស្រាក ដែល ១០១០ នៃការ ដែល ១០ នេះបា

ത്താരുട്ട് ത്രാരണത്താര്യ the identifying a secondidata/input terminal of the programmable routing. 💎 📑 വരുന്ന് ത്രദ etials and to an incommultiplexer, wherein a selection between the first and second data input terminals is determined by a value stored in a memory cell controlling the programmable routing multiplexer, and

> routing the node on a second routing path between the first and second logic blocks, wherein the second routing path traverses the programmable routing multiplexer via the second data input terminal.

21. (Withdrawn) The computer system of Claim 20, further comprising an evaluation module for evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.

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22. (Currently Amended) A method of implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the method comprising:

identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer;

routing a node in the design to the first data input terminal; and routing the node to the second data input terminal:

23. (Currently Amended) The method of Claim 22, further comprising:

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கண்ணைகள் கண்டு in arouting the node to the third data fingut terminal fice நீன்ற நின்ற நடித்த நடித்த கண்டிய மு

இது நிறுக்கின் . . . 24: (Original) The method of Claim 22, wherein the BLD is a field:programmable gate எர்க்கு நடித்த array (FPGA).

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- 25. (Original) The method of Claim 24, wherein the first and second memory cells are static RAM-based configuration memory cell of the FPGA.
- 26. (Original) The method of Claim 22, wherein the multiplexer is a 4-to-1 multiplexer.
- 27. (Original) The method of Claim 22, further comprising:

evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.

28. (Currently Amended) A computer-readable storage medium comprising computer-executable code for implementing a design in a programmable logic device (PLD) to reduce susceptibility to single-event upsets (SEUs), the medium comprising:

code for identifying in a programmable routing multiplexer of the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined <u>solely</u> by a first value stored in a first memory cell controlling the programmable routing multiplexer; and

code for routing a node in the design to both of the first and second data input terminals.

ான நாள் அவர் 29. (Original) The computer-readable storage medium) of Claim 28, further comprising டி. டி. டி. அது சார்கள் அம்மாக code for evaluating the node and determining that the node is not included imadriple உண்கள் கொள்க சி. டி. இ தேத்து அது கார்கள் amodular redundancy (TMR) circuit. உள்ள கார்கள் அதித்து கார்கள் கொள்க கார்கள் அது சி. இது க

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gssegnant and 30. (Currently Amended). A computer system for implementing a design in a பொரு கொள்ள பிருக்க பிர காண் காகில் programmable logic device (PLD) to reduce susceptibility to single-event upsets வகையில் பிருக்கிய வ காதத்தார் அது (SEUs), the computer system comprising வகியின்ன மண்ணையை செய்ய கிறிய கொள்ள மாகிய முற

the PLD a first data input terminal and a second data input terminal, wherein a selection between the first and second data input terminals is determined solely by a first value stored in a first memory cell controlling the programmable routing multiplexer; and

a routing module for routing a node in the design to both of the first and second data input terminals.

31. (Original) The computer system of Claim 30, further comprising an evaluation module for evaluating the node and determining that the node is not included in a triple modular redundancy (TMR) circuit.